## REMARKS

Claims 6, 7, 9, 11-13 and 15-19 are pending in the present application. Claim 6 has been amended.

## Claim Rejections-35 U.S.C. 112

Claims 6, 7, 9, 11-13 and 15-19 have been rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description requirement. The Examiner has asserted that the protective layer of the claims "having substantially uniform thickness" was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor, at the time the application was filed, had possession of the claimed invention. This rejection is respectfully traversed for the following reasons.

Applicant initially emphasizes that claim 6 for example features in combination that the protective layer has "substantially uniform thickness". As described beginning on page 11, line 18 of the present application with respect to Fig. 1(e), a chemical mechanical polishing (CMP) is used to flatten a rugged portion of the surface, whereby silicon nitride layer 33 is used as a CMP stop. Accordingly, polysilicon layer 12 after CMP processing would inherently have "substantially" uniform thickness. That is, the description of forming the protective layer by CMP so as to leave the polysilicon as a protective layer at a portion which is open to the nitride layer, as shown in Fig. 1(e) of the present application, should enable one of ordinary skill in the art to understand that

the thickness of the protective layer is substantially uniform. Regardless of the variables as suggested by the Examiner, since the protective layer is planarized, the protective layer should be understood as having substantially uniform thickness, although not exactly. Applicant therefore respectfully submits that the specification provides written description so as to reasonably convey that Applicant had possession of the claimed invention, and that claims 6, 7, 9, 11-13 and 15-19 are thus in compliance with 35 U.S.C. 112, first paragraph. The Examiner is therefore respectfully requested to withdraw this rejection for at least these reasons.

**Claim Rejections-35 U.S.C. 102**

Claims 6, 7, 9, 11-13 and 15-19 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Yoo et al. reference (U.S. Patent No. 5,605,853). This rejection is respectfully traversed for the following reasons.

The semiconductor device of claim 6 includes in combination first and second gates; a field oxide; a protective layer "formed directly on said field oxide to prevent overetching of said field oxide, said protective layer being a conductive layer, having side surfaces thereof over said field oxide, and having substantially uniform thickness"; sidewall spacers; and an insulating layer, a contact hole and a connecting wire. Applicant respectfully submits that the Yoo et al. reference as relied upon does not disclose these features.

The Examiner has interpreted floating gate 21 in Fig. 7 of the Yoo et al.

reference as the protective layer of claim 6. However, as described beginning in column 3, line 64 of the Yoo et al. reference, a first layer of polycrystalline silicon is deposited, and the polysilicon is patterned by conventional lithography and etching to form gate electrodes 16, polysilicon interconnect 16' and floating gate 21. Since floating gate 21 of the Yoo et al. reference is formed by conventional lithography and etching, and is not flattened or planarized, floating gate 21 does not have substantially uniform thickness, and thus cannot be interpreted as the protective layer of claim 6. Applicant therefore respectfully submits that the semiconductor device of claim 6 distinguishes over the Yoo et al. reference as relied upon by the Examiner, and that this rejection of claims 6, 7 and 9, is improper for at least these reasons.

Independent claims 11 and 16 both respectively feature in combination a protective layer "formed directly on said field oxide to prevent overetching of said field oxide, said protective layer being a conductive layer, having side surfaces thereof over said field oxide, and having substantially uniform thickness". As emphasized previously, floating gate 21 in Fig. 7 of the Yoo et al. reference is patterned by conventional lithography and etching. Since floating gate 21 of the Yoo et al. reference is formed by conventional lithography and etching, and is not flattened or planarized, floating gate 21 does not have substantially uniform thickness, and thus cannot be interpreted as the protective layers of respective claims 11 and 16. Applicant therefore respectfully submits that the semiconductor devices of respective claims 11 and 16 distinguish over the Yoo et al. reference as relied upon by the Examiner, and that this

rejection of claims 11-13 and 15-19, is improper for at least these reasons.

## Conclusion

The Examiner is respectfully requested to enter this Amendment. Claim 6 has been amended merely to correct a misspelling. Entry of this Amendment thus would not require further consideration and/or search, and would not raise new issues.

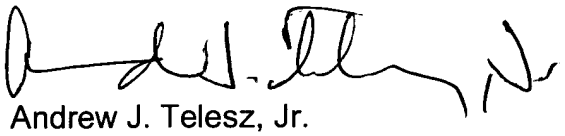
The Examiner is further respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740